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ELPENORD, CANDAL	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/804,674	VARMA, ANUJAN	
	Examiner	Art Unit	
	Candal Elpenord	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 November 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13 and 19-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13 and 19-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *See Continuation Sheet*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-13, 19-36 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. **Claims 1, 5-11** are rejected under 35 U.S.C. 102(e) as being anticipated by Sakamoto et al (US 6,836,479 B1).

Claims 1, 5-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Antal et al (US 7,224,703 B2) in view of.

Regarding claim 1, Sakamoto et al. discloses a switching device (fig. 1, Core Switch 101, recited in cool. 4, lines 41-52) comprising a segmentation unit (fig. 1, Input Interface 3, "segments variable length packet into fixed length cells", recited in col. 2, lines 39-46) to receive data packets of variable size ("interface stores of packets in col. 3, lines 1-8) and to store the data packets as segments (fig. 1, Input Interface 3-1, Queue 65-

1-2, recited in col. 3, lines 15-24), wherein the data packets received having a length greater than a maximum segment length variable length packets can be of many sizes) are divided into multiple segments (fig. 1, Input Interface 3, "segments variable length packet into fixed length cells", recited in col. 2, lines 39-46) a plurality of queues to store the segments (fig. 1, Corresponding queues 65-1-2, recited in col. 5, lines 2-12, "input Interface with plurality of queues to stores the packets", recited in col. 3, lines 15-23, fig. 1, Lower queues 67 where the cells are stored as segments, recited in col. 6, lines 6-15), wherein the queues ("plurality of queues corresponding to output interfaces", recited in col. 3, lines 15-23) are associated with destinations (fig. 1, Output Interface 4-1, 4-n, recited in col. 4, lines 65- col. 5, lines 6); a scheduler (fig. 21, Scheduler 61, recited in col. 6, lines 34-43) to generate a schedule ("scheduler commands the crossbar switch to turn contact ('switches the packets"), recited in col. 6, lines 34-46) including a data path from at least one queue (fig. 1, Corresponding queue 65-1-2, recited in col. 5, lines 2-12, fig. 21, Input Buffer 121, recited in col. 6, lines 34-43) to an associated destination (fig. 1, Output Interface 4-1, recited in col.5, lines 2-13); a framer ("variable communication device reassemble the cells into the packet", recited in col. 2, lines 59-63) to aggregate a plurality of segments to form a frame, (fig. 13, Cells 67 as the segments, recited in cool. 23-30, "the cells segments from the arriving packets", recited in col. 6, lines 25-28); wherein the frame has a maximum frame length (fig. 13, Cells 67 as the segments, recited in cool. 23-30, "the cells segments from the arriving packets", recited in col. 6, lines 25-28), wherein the segments are retrieved ("taking of packets from the container where they are reassembled", recited in col. 3, lines 4-11) from the at least one queue ("output Interface with packet reassembling buffers corresponding to input interfaces", recited in

col. 3, lines 24-29), and wherein the frame may contain segments (fig. 13, Cells 67 as the segments, recited in cool. 23-30, "the cells segments from the arriving packets", recited in col. 6, lines 25-28) associated with different data packets (fig. 5, Packet in container A and Container B, recited in col. 9, lines 25-35) ; and a transmitter ("output Interface takes the packet and transmits it to transmission path", recited in col. 3, lines 7-11) to transmit the frame to the associated destination ("transmission of cell from input interface to output interface", recited in col. 6, lines 23-25), wherein the segments (fig. 13, Cells 67 as the segments, recited in cool. 23-30, "the cells segments from the arriving packets", recited in col. 6, lines 25-28) within the frame are transmitted together ("parallel transmission", recited in co. 6, lines 31-35) and a switch fabric (fig. 1, Cell Switch 62 composed of crossbar switch 2, recited in col. 5, lines 1-5) to provide a configurable connection (fig. 1, Cell Switch 62, Setting up a path between input interface and the output interface", recited in col. 6, lines15-22) between a plurality of sources (fig. 1, Input Interfaces 3-1, 3-n, recited in col. 4. lines 65- col. 5, lines 5) and a plurality of destinations (fig. 1, Output Interfaces 4-1. 4-n, recited in col. 5, lines 1-5) , wherein said switch fabric (fig. 1, Cell Switch 62 composed of crossbar switch, recited in col. 5, lines 1-5, fig. 21, Cell Switch 62) is configured ("scheduler 61, "commands the crossbar switch", recited in col. 6, lines 34-42, fig. 2, "From Scheduler 61 to Cell Switch 62) by said scheduler (fig. 21, Scheduler 61, recited in col. 6, lines 34-43) and wherein said switch fabric (fig. 1, Cell Switch 62 composed of crossbar switch, recited in col. 5, lines 1-5, fig. 21, Cell Switch 62) transmits frames from at least a subset of the plurality of sources ("crossbar switch performs transmission in parallel, set different paths simultaneously", recited in col. 6, lines 29-33) to at least a subset of the plurality of

destinations (fig. 1, Output Interfaces 4-1. 4-n, recited in col. 5, lines 1-5) during a schedule cycle ("predetermined scheduling system by the scheduler", recited in col. 9, lines 53-55).

Regarding claim 5, the device (fig. 1, Packet Switch.Communication switch, recited in col. 4, lines 65 -col. 5, lines 5), wherein said scheduler (fig. 21, Scheduler 61, recited in col. 6, lines 34-39) generates the schedule ("the scheduler instructs which output interface may transmit", recited in col. 9, lines 40-52) based on requests (fig. 6, Transmission Request 50, recited in col. 9, lines 40-52) for data packets ("the scheduler indicates packets to be transmitted based on requests", recited in col. 7, lines 44-51) from particular queues (fig. 21, Output buffers 122, recited in col. 7, lines 24-27) to be transmitted to particular destinations (fig. 21, Output Interface 4, recited in col. 7, lines 38-51).

Regarding claim 6, the device (fig. 1, Packet Switch Communication switch, recited in col. 4, lines 65 -col. 5, lines 5), wherein the wherein said scheduler (fig. 21, Scheduler 61, recited in col. 6, lines 34-39) matches the requests and resolves conflicts in order to generate the schedule ("scheduler transmits packets with high priority when there are a plurality of transmissions requests from a plurality of input interfaces to output interfaces", recited in col. 6, lines 43-48).

Regarding claim 7, the device (fig. 1, Packet Switch Communication switch, recited in col. 4, lines 65 -col. 5, lines 5), wherein said plurality of queues (fig. 2, Queue-1H, Queue-1L, "queues corresponding to priority", recited in col. 7, lines 58- col. 8, lines 4) include one or more queues (see, "n as the number of output queues at the output interface", recited in col. 7, lines 58 –col. 8, lines 4) per destination ("packet with high

priority to be transmitted to output interface 1", recited in col. 7, lines 58- col. 8, lines 4) based on priorities associated with the destinations ("candidates for output packet being decided with priority", recited in col. 5, lines 5-19).

Regarding claim 8, the device fig. 1, Packet Switch Communication switch, recited in col. 4, lines 65 -col. 5, lines 5) wherein said framer ("variable communication device", recited in col. 2, lines 59-65) forms the frame by aggregating segments ("reassemble of cells", recited in col. 6, lines 25-33)from some subset of the one or more associated queues (see, "n as the number of output queues at the output interface", recited in col. 7, lines 58 –col. 8, lines 4).

Regarding claim 9, the device fig. 1, Packet Switch Communication switch, recited in col. 4, lines 65 -col. 5, lines 5), wherein said framer ("variable communication device", recited in col. 2, lines 59-65) forms the frame by aggregating complete segments ("reassemble of cells", recited in col. 2, lines 59-62).

Regarding claim 10, the device (fig. 1, Packet Switch Communication switch, recited in col. 4, lines 65 -col. 5, lines 5), wherein said framer ("variable communication device", recited in col. 2, lines 59-65) pads the frame to reach the maximum frame length ("insertion of pad if the packet is not as long as the cell length", recited in col. 5, lines 25-30).

Regarding claim 11, the device(fig. 1, Packet Switch Communication switch, recited in col. 4, lines 65 -col. 5, lines 5), wherein said transmitter ("transmission of cells", recited in col. 2, lines 51-55) transmits the segments (fig. 13, Cells 67 as the segments, recited in cool. 23-30, "the cells segments from the arriving packets", recited

in col. 6, lines 25-28) making up a particular data packet in order ("arrival order", recited in col. 2, lines 58-63).

4. **Claims 19, 21, 24-25, 34** are rejected under 35 U.S.C. 102(b) as being anticipated by Moriwaki et al (US 6,999, 413 B2).

Regarding claims 19, Moriwaki et al (US 6,999,413) discloses an apparatus (fig. 1, Packet Switched Communication Apparatus, recited in col. 6, lines 17-27) comprising a plurality of sources (fig. 1, Input Line Interfaces 40-1, 40-n, recited in col. 6, lines 17-32); a plurality of destinations (fig. 1, Line Interfaces 20-1, 20-n, recited in col. 6, lines 17-27); a receiver to receive frames ("Line Interfaces receiving the fixed length blocks", recited in col. 6, lines 17-32), wherein the frames ("fixed length blocks", recited in col. 6, lines 17-32) include a plurality of segments and the segments may be associated with multiple data packets (fig. 4, plurality of variable length packets, recited in col. 7, lines 21-30); a deframer (fig. 8, ARB-ACK Extractor 36, "extracting from the block", recited in col. 9, lines 35-45) to extract the segments from the frame ("extracting from the block and regenerating", recited in col. 9, lines 48 – col. 10, lines 7); a queue (fig. 3, Queue 23-1, recited in col. 7, lines 7-20) to store the segments ("variable lengths are divided and stored in a queue", recited in col. 7, lines 7-20); a state monitor to track complete packets contained within the queue ("detecting boundaries of variable length packets", recited in col. 10, lines 8-24); a reassembly unit (fig. 3, Packet Regenerating VIQ 33-1-33-n, recited in col. 9, lines 55- col. 10, lines 7) to combine the segments making up a complete packet together to generate the packet (fig. 3, Packet Regenerating VIQ 33-1-33-n, recited in col. 9, lines 55- col. 10, lines 7); a scheduler (fig. 1, Scheduler 11, recited in col. 6, lines 29-

41) to generate a schedule for transmitting frames ("the scheduler decides the optimum input/output connections by schedule algorithm", recited in col. 9, lines5-13) ; and a switch fabric (fig. 1, Crossbar Switch (nxn)10, recited in col. 6, lines 17-41) to selectively connect ("deciding connection relationship", recited in col. 6, lines 32-35) the plurality of sources (fig. 1, Input Line Interfaces 40-1, 40-n, recited in col. 6, lines 17-32) to the plurality of destinations (fig. 1, Line Interfaces 20-1, 20-n, Output Line 50-1, 50-n, recited in col. 6, lines 17-27) based on the schedule ("crossbar switches in response to signals from the scheduler", recited in abstract, lines 1-8), wherein said switch fabric (fig. 1, Crossbar Switch (nxn) 10, recited in col. 6, lines 17-41) transmits frames ("each interface line distributes fixed length blocks", recited in col. 6, lines 32-41, "interface outputs packets gathered in blocks", recited in col. 4, lines 5-15, "switching of incoming blocks to corresponding output ports", recited in col. 8, lines 58-62) from at least a subset of the plurality of sources (fig. 1, Input Line Interfaces 40-1, 40-n, recited in col. 6, lines 17-32) to at least a subset of the plurality of destinations (fig. 1, Line Interfaces 20-1, 20-n/Output Line 50-1, 50-n, recited in col. 6, lines 17-27).

Regarding claim 21, the apparatus (fig. 1, Packet Switched Communication Apparatus, recited in col. 6, lines 17-27), further comprising an error checker (fig. 2A, Layer 2 Controller 21-3, recited in col. 6, lines 52-60) to check for errors in the frame (fig. 2A, Layer 2 controller 21-3, "performs error check", recited in col. 6, lines 52-60).

Regarding claim24, Moriwaki et al. disclose a method (fig. 1, Packet Communication Apparatus, recited in col. 6, lines 17-27) comprising receiving frames of data ("Line Interfaces receiving the fixed length blocks", recited in col. 6, lines 17-32) from a plurality of sources (fig. 1, Input Line Interfaces 40-1, 40-n, recited in col. 6, lines

17-32) for a plurality of destinations (fig. 1, Line Interfaces 20-1, 20-n/Output Line 50-1, 50-n, recited in col. 6, lines 17-27) over a switch fabric (fig. 1, Crossbar Switch (nxn) 10, recited in col. 6, lines 17-41), wherein a frame includes a plurality of segments (fig. 4, block 1(200-1), block 2 (200-2) of variable length packets 100A to 100E, recited in col. 7, lines 21-26), and wherein the frames (fig. 4, block 1(200-1), block 2 (200-2) of variable length packets 100A to 100E, recited in col. 7, lines 21-26) and wherein the segments (fig. 4, block 1(200-1), block 2 (200-2) of variable length packets 100A to 100E, recited in col. 7, lines 21-26), and wherein the frames (fig. 4, block 1(200-1), block 2 (200-2) of variable length packets 100A to 100E, recited in col. 7, lines 21-26) may be associated with multiple data packets (fig. 4, plurality of variable length packets, recited in col. 7, lines 21-30); extracting the segments from the frame ("extracting from the block and regenerating", recited in col. 9, lines 48 – col. 10, lines 7); storing the segments in a queue (fig. 4, see, combining of incoming packets, recited in col. 7, lines 22-26, "variable lengths are divided and stored in a queue", recited in col. 7, lines 7-20); monitoring complete packets ("detecting boundaries of variable length packets", recited in col. 10, lines 8-24) contained within the queue ("boundaries can be decide according to the length information", recited in col. 10, lines 26); and combining the segments making up a complete packet together to generate the packet (fig. 3, Packet Regenerating VIQ 33-1-33-n, recited in col. 9, lines 55- col. 10, lines 7, "regenerating of packet from the fixed length blocks", recited in col. 10, lines 8-19).

Regarding claim 25, the method (fig. 1, Packet Switched Communication Apparatus, recited in col. 6, lines 17-27), further comprising checking for errors(fig. 2A,

Layer 2 Controller 21-3, recited in col. 6, lines 52-60) in the frame (fig. 2A, Layer 2 controller 21-3, "performs error check", recited in col. 6, lines 52-60).

Regarding claim 34, Moriwaki et al. discloses a store and forward device (fig. 1, Packet Communication Apparatus, recited in col. 6, lines 17-27) comprising a plurality of ingress interface modules (fig. 1, Line I/F #1, Line I/F #n, recited in col. 6, lines 17-27) to receive packets of variable size ("incoming variable length packets", recited in col. 6, lines 17-27), store the packets as segments (fig. 4, see, combining of incoming packets, recited in col. 7, lines 22-26, "variable lengths are divided and stored in a queue", recited in col. 7, lines 7-20); in queues (fig. 3, Queues 23-1, 23-n recited in col. 7, lines 7-20), aggregate multiple segments ("joining of data packets", recited in col. 6, lines 35-41) together to form a frame ("regenerating of packet from the fixed length blocks", recited in col. 10, lines 8-19), and transmit (fig. 3, Block Distributor 22, recited in col. 6, lines 42-47) the segments within the frame together ("each interface line distributes fixed length blocks", recited in col. 6, lines 32-41, "interface outputs packets gathered in blocks", recited in col. 4, lines 5-15, "switching of incoming blocks to corresponding output ports", recited in col. 8, lines 58-62), wherein the segments stored in the queues have a segment maximum size and the packets (fig. 4, plurality of variable length packets, recited in col. 7, lines 21-30-variable length packets can have multiple sizes) having a larger size ("incoming variable length packets", recited in col. 6, lines 17-27-variable length packets can be of multiple sizes) are divided ("divide of variable length packets", recited in col. 7, lines 21-29) into multiple segments (fig. 4, block 1(200-1), block 2 (200-2) of variable length packets 100A to 100E, recited in col. 7, lines 21-26),

and wherein the frames (fig. 4, block 1(200-1), block 2 (200-2) of variable length packets 100A to 100E, recited in col. 7, lines 21-26) have a maximum frame size and include a plurality of whole segments and may include segments (fig. 4, block 1(200-1), block 2 (200-2), recited in col. 7, lines 21-26) associated with different packets (fig. 4, plurality of variable length packets such as 100A to 100E, recited in col. 7, lines 21-30); a plurality of egress interface modules (fig. 1, Egress Interface 20-1, 20-n, recited in col. 6, lines 17-29) to receive frames ("Line Interfaces receiving the fixed length blocks", recited in col. 6, lines 17-32), divide the frames (fig. 3, Elements 23, 24, 27 as the framer that forms the frames form the packet blocks into segments ("blocks", recited in col. 7, lines 34-41), store the segments in queues ("stored variable length packet in block generating queue (VOQ 23-1, 23-n), recited in col. 7, lines 11-17, "store of packet block in packet regenerating VIQ-virtual Input Queue, recited in col. 57-60), monitor ("detecting boundaries of variable length packets", recited in col. 10, lines 8-24) the queues for complete packets ("boundaries can be decide according to the length information", recited in col. 10, lines 26) and reassemble a packet after the segments making up the packet are received ("packets regenerating so variable length packet can be obtained form fixed length blocks stored in the queue buffer", recited in col. 10, lines 8-17); a switching matrix (fig. 1, Crossbar Switch (nxn)10, recited in col. 6, lines 17-41) to provide selective connectivity ("connection relationship between input and output ports", recited in col. 6, lines 32-35) between said plurality of ingress interface modules (fig. 1, Ingress/ Line I/F #1, Line I/F #n, recited in col. 6, lines 17-27) and said plurality of egress interface modules (fig. 1, Egress Interface 20-1, 20-n, recited in col. 6, lines 17-29); a backplane (fig. 1, fig. 11, "crossbar switching planes 10-1 to 10-5", recited in col.

9, lines 14-21) consisting of a plurality of channels (fig. 1, Connection Links 41-1-x to 41-5-x, recited in col. 6, lines 35-41) to connect said plurality of ingress interface modules (fig. 1, Ingress/ Line I/F #1, Line I/F #n, recited in col. 6, lines 17-27) and said plurality of egress interface modules (fig. 1, Egress Interface 20-1, 20-n, recited in col. 6, lines 17-29) to said switching matrix (fig. 1, Crossbar Switch (nxn)10, recited in col. 6, lines 17-41); and a scheduler (fig. 1, Scheduler 11, recited in col. 6, lines 29-41) to select connectivity ("the scheduler decides the optimum input/output connections by schedule algorithm", recited in col. 9, lines5-13) between said plurality of ingress interface modules (fig. 1, Ingress/ Line I/F #1, Line I/F #n, recited in col. 6, lines 17-27) and said plurality of egress interface modules (fig. 1, Egress/ Line Interfaces 20-1, 20-n, recited in col. 6, lines 17-27), and to configure ("deciding connection relationship", recited in col. 6, lines 32-35) said switching matrix accordingly (fig. 1, Crossbar Switch (nxn)10, recited in col. 6, lines 17-41).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.

2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. **Claims 2-4, 12** are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto et al (US 6,836,479 B1). In view of Antal et al (US 7,224,703 B2).

Regarding claim 2-4, 12, Sakamoto et al. disclose the device fig. 1, Packet Switch Communication switch, recited in col. 4, lines 65 -col. 5, lines 5). Sakamoto et al . discloses all the claimed invention with the exception of being silent with respect to the following features: **regarding claim 2**, wherein said segmentation unit divides the data packets having a length greater than the maximum segment length to form at least a first segment having the maximum segment length, **regarding claim 3**, wherein a last segment formed by said segmentation unit may be less than the maximum segment length; **regarding claim 4**, wherein said segmentation unit identifies a final segment belonging to a particular data packet, **regarding claim 12**, wherein the transmitter interleaves segments with different packets.

However, Antal et al (US 7,224,703 B2) in a similar field of endeavor discloses: **regarding claim 1**, wherein the frame has a maximum frame length (fig. 3, Size of Maximal segment, recited in col. 2, lines 44-48, fig. 2C Segment 4 as the larger segment among the segments, recited in col. , **regarding claim 2**, wherein said segmentation unit (fig.4, Segmenter 22, recited in col.4, lines 55-63) divides the data packets having a length greater than the maximum segment length ("data packet segmented into plural segments", recited in col. 3, lines 26-35, fig. 3, "size of largest segment of a 1013 byte packet", recited in col. 2, lines 44-48) to form at least a first segment having the

maximum segment length ('setting the first segment to a size larger than the maximal segment size", recited in col. 6, lines 55-62), **regarding claim 3**, wherein a last segment ("last segment", recited in col. 3, lines 39-42) formed by said segmentation unit (fig.4, Segmenter 22, recited in col.4, lines 55-63) may be less than the maximum segment length ('the last segment is the same size as the first segment whose less than the maximal segment size", recited in col.. 3, lines 33-42); **regarding claim 4**, wherein said segmentation unit (fig.4, Segmenter 22, recited in col.4, lines 55-63) identifies a final segment belonging to a particular data packet ("smaller packet making up the last packet segment", recited in col. 1, lines 62- col. 2, line 1), **regarding claim 12**, wherein the transmitter interleaves segments associated with different data packets ("the scheduler multiplexes the priority 1 traffic with packet segments from lower priority level traffic and sends to physical channel/link", recited in col. 8, lines 5-12). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the features of Sakamoto et al. by using features as taught by Antal et al. in order to reduce transmission delay of high priority traffic.

8. **Claim 13** is rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto et al (US 6,836,479 B1) in view of Beshai et al (US 7,233,590).

Sakamoto et al. discloses the device as recited in above paragraph. However, Sakamoto et al. is silent with respect to a striper to striper the frame across a plurality of channels.

However, Beshai et al. in the same field of endeavor discloses a striper to striper the frame across a plurality of channels ("frame is striped across an entire link", recited in abstract, lines 6-12, where the entire link constitutes a plurality of channels, recited in col.

4, lines 36-43). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the features of Sakamoto et al. with Antal et al. by using features as taught by Beshai et al. in order to provide accommodation to data streams of high rates (See Col. 2, lines 52-64 for motivation).

9. **Claim 20** is rejected under 35 U.S.C. 103(a) as being unpatentable over Moriwaki et al (US 6,999,413 B2) in view of Lay et al (US 6,862,293 B2).

Regarding claim 20, Moriwaki et al. discloses the apparatus (fig. 1, Packet Communication Apparatus, recited in col. 6, lines 17-27).

Moriwaki et al. teaches all the claimed invention with the exception of being silent with regard to the following features: wherein the frames are striped over a plurality of channels and said receiver is a deskewer that receives the frame over the plurality of channels and deskews the stripes and combines them into the frame.

However, Lay et al in a similar field of endeavor discloses: the frames (fig. 2, FDI 205, "lanes of stripe data", recited in col. 4, lines 26-34) are striped over a plurality of channels ("spread across plural lanes", recited in col. 4, lines 35-43) and said receiver (fig. 2, Blocks 295, recited in col. 5, lines 1-9) is a deskewer ("lane deskew", recited in col. 5, lines 1-9) that receives the frame over the plurality of channels ("plural lanes", recited in col. 4, lines 35-43) and deskews the stripes and combines them into the frame ("deskew and alignment on the receive side", recited in col. 5, lines 1-9). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the features of Moriwaki et al. by using features as taught by Lay et al. in order to provide high speed link aggregations (See Col. 2, lines 45-65 for motivation).

10. **Claim 22** is rejected under 35 U.S.C. 103(a) as being unpatentable over Moriwaki et al (US 6,99,413 B2) in view of Moriwaki et al (US 7,212,525 B2).

Moriwaki(413) et al. discloses the apparatus (fig. 1, Packet Switched Communication Apparatus, recited in col. 6, lines 17-27), the error-checker to check for errors in frame as recited in above paragraph.

Moriwaki et al (413 B2) discloses all the claimed limitation with the exception of the following features: wherein said error checker checks for errors by comparing a grant received to the frame.

However, Moriwaki et al (525 B2) in the same field of endeavor discloses: wherein said error checker checks for errors by comparing a grant ("validity identification of grants" recited in col. 6, lines 21-32) received to the frame ("granted packets in the buffer", recited in col. 6, lines 8-14). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the features of Moriwaki et al (413 B2) by using features as taught by Moriwaki et al (525 B2) in order to provide validity identification of grants (see Col. 3, lines 1-14 for motivation).

11. **Claim 23** is rejected under 35 U.S.C. 103(a) as being unpatentable over Moriwaki et al (US 6,99413 B2) in view of Davidson et al (US 6,804,692 B2).

Regarding claim 23, Moriwaki et al. discloses the (fig. 1, Packet Switched Communication Apparatus, recited in col. 6, lines 17-27).

However, Moriwaki et al. is silent with respect to wherein the state monitor determines completes packets by detecting an end of packet.

Davidson et al. in the same field of endeavor discloses wherein the state monitor (fig. 1, Preprocessor 12, recited in col.3, lines 27-35) determines complete packets ("examining of data blocks to determine complete packet", recited in col. 7, lines 24-34) by detecting an end of packet (fig. 3B, EOO as end of packet, recited in col. 7, lines 53—col. 8, lines 6). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the features of Moriwaki et al. by using the features as taught by Davidson et al. in order to provide blocks reassembly by assigning a unique identifier to each block (See col. 1, lines 65- col. 2, lines 6 for motivation).

12. **Claims 27-30, 32-33** are rejected under 35 U.S.C. 103(a) as being unpatentable over Moriwaki et al (US 6,999,413 B2) in view of Sakamoto et al (US 6,836479 B1).

Regarding claim 27, Moriwaki et al. disclose a store and forward device (fig. 1, Packet Switched Communication Apparatus, recited in col. 6, lines 17-27) comprising a plurality of Ethernet cards (fig. 1, Input Lines 40-1, 40-n, Output Lines 50-1, 50-n, recited in col. 6, lines 17-29) to receive data from ("receiving of variable length packets", recited in col. 6, lines 23-29) and transmit data ("routing processing of variable length packets", recited in col. 6, lines 23-29) to external sources (fig. 1, Line Interfaces 20-1, 20-n, recited in col. 6, lines 17-25) , wherein the plurality of Ethernet cards (fig. 1, Input Lines 40-1, 40-n, Output Lines 50-1, 50-n, recited in col. 6, lines 17-29) include an ingress interface module (fig. 1, Line I/F #1, Line I/F #n, recited in col. 6, lines 17-27) to receive packets of variable size ("receiving of variable length packets", recited in col. 6, lines 23-29), store the packets as segments (fig. 4, see, combining of incoming packets,

recited in col. 7, lines 22-26, "variable lengths are divided and stored in a queue", recited in col. 7, lines 7-20) in queues (fig. 1, Virtual Output Queues at line I/F #1 and Line I/F #n) associated with at least some subset of destination (fig. 1, Line Interfaces 20-1, 20-n, recited in col. 6, lines 17-27) and priority, aggregate multiple segments ("joining of data packets", recited in col. 6, lines 35-41) together to form a frame, and transmit the segments within the frame together ("each interface line distributes fixed length blocks", recited in col. 6, lines 32-41, "interface outputs packets gathered in blocks", recited in col. 4, lines 5-15, "switching of incoming blocks to corresponding output ports", recited in col. 8, lines 58-62), wherein the segments stored in the queues ("stored variable length packet in block generating queue (VOQ 23-1, 23-n), recited in col. 7, lines 11-17, "store of packet block in packet regenerating VIQ-virtual Input Queue, recited in col. 57-60) have a segment maximum size (fig. 4, plurality of variable length packets, recited in col. 7, lines 21-30-variable length packets can have multiple sizes and the packets having a larger size (fig. 4, plurality of variable length packets, recited in col. 7, lines 21-30-variable length packets can have multiple sizes) are divided into multiple segments ("divide of variable length packets", recited in col. 7, lines 21-29) into multiple segments (fig. 4, block 1(200-1), block 2 (200-2) of variable length packets 100A to 100E, recited in col. 7, lines 21-26), and wherein the frames (fig. 4, block 1(200-1), block 2 (200-2) of variable length packets 100A to 100E, recited in col. 7, lines 21-26) have a maximum frame size, include a plurality of segments (fig. 4, Block 1, Block 2 as the plurality of segments, recited in col. 7, lines 21-26) and may include segments (fig. 4, Block 1, Block 2 as the plurality of segments, recited in col. 7, lines 21-26) associated with different packets (fig. 4, plurality of variable length packets such as 100A to 100E, recited in col.

7, lines 21-30); and an egress interface module (fig. 1, Egress Interface 20-1, 20-n, recited in col. 6, lines 17-29) to receive frames ("Line Interfaces receiving the fixed length blocks", recited in col. 6, lines 17-32), divide the frames into segments (fig. 3, Elements 23, 24, 27 as the framer that forms the frames from the packet blocks into segments ("blocks", recited in col. 7, lines 34-41), store the segments in a queue, monitor ("detecting boundaries of variable length packets", recited in col. 10, lines 8-24) the queues for complete packets , and reassemble a packet after the segments making up the packet are received ("packets regenerating so variable length packet can be obtained form fixed length blocks stored in the queue buffer", recited in col. 10, lines 8-17); a switching matrix (fig. 1, Crossbar Switch (nxn)10, recited in col. 6, lines 17-41) to provide selective connectivity ("deciding connection relationship", recited in col. 6, lines 32-35) between said Ethernet cards (fig. 1, Input Lines 40-1, 40-n, Output Lines 50-1, 50-n, recited in col. 6, lines 17-29); a backplane (fig. 1, fig. 11, "crossbar switching planes 10-1 to 10-5", recited in col. 9, lines 14-21) consisting of a plurality of channels (fig. 1, Connection Links 41-1-x to 41-5-x, recited in col. 6, lines 35-41) to connect said plurality of Ethernet cards (fig. 1, Input Lines 40-1, 40-n, Output Lines 50-1, 50-n, recited in col. 6, lines 17-29) to said switching matrix (fig. 1, Crossbar Switch (nxn)10, recited in col. 6, lines 17-41); and a scheduler (fig. 1, Scheduler 11, recited in col. 6, lines 29-41) to select connectivity ("connection relationship between input and output ports", recited in col. 6, lines 32-35) between Ethernet cards (fig. 1, Input Lines 40-1, 40-n, Output Lines 50-1, 50-n, recited in col. 6, lines 17-29); and to configure said switching matrix accordingly (fig. 1, Crossbar Switch (nxn)10, recited in col. 6, lines 17-41); **regarding claim 28**, the device (fig. 1, Packet Switched Communication Apparatus, recited in col.

6, lines 17-27), wherein said backplane (fig. 1, fig. 11, "crossbar switching planes 10-1 to 10-5", recited in col. 9, lines 14-21) also connects said plurality of Ethernet cards (fig. 1, Input Lines 40-1, 40-n, Output Lines 50-1, 50-n, recited in col. 6, lines 17-29) to said scheduler (fig. 1, Scheduler 11, recited in col. 6, lines 29-41); **regarding claim 29**, the device (fig. 1, Packet Switched Communication Apparatus, recited in col. 6, lines 17-27), wherein said backplane (fig. 1, fig. 11, "crossbar switching planes 10-1 to 10-5", recited in col. 9, lines 14-21) uses same channels (fig. 1, Connection Links 41-1-x to 41-5-x, recited in col. 6, lines 35-41) to connect said Ethernet cards (fig. 1, Input Lines 40-1, 40-n, Output Lines 50-1, 50-n, recited in col. 6, lines 17-29) to said switching matrix (fig. 1, Crossbar Switch (nxn)10, recited in col. 6, lines 17-41); and to said scheduler; **regarding claim 30**, the device (fig. 1, Packet Switched Communication Apparatus, recited in col. 6, lines 17-27), wherein said backplane (fig. 1, fig. 11, "crossbar switching planes 10-1 to 10-5", recited in col. 9, lines 14-21) provides a logical separation of data path ("allocation of time slot corresponding to n crossbar switches", recited in col. 4, lines 9-15) between said Ethernet cards (fig. 1, Input Lines 40-1, 40-n, Output Lines 50-1, 50-n, recited in col. 6, lines 17-29) and said switching matrix (fig. 1, Crossbar Switch (nxn)10, recited in col. 6, lines 17-41) and scheduling path between said Ethernet cards (fig. 1, Input Lines 40-1, 40-n, Output Lines 50-1, 50-n, recited in col. 6, lines 17-29) and said scheduler (fig. 1, Scheduler 11, recited in col. 6, lines 29-41); **regarding claim 32**, the device (fig. 1, Packet Switched Communication Apparatus, recited in col. 6, lines 17-27), wherein the backplane (fig. 1, fig. 11, "crossbar switching planes 10-1 to 10-5", recited in col. 9, lines 14-21) is optical (fig. 2B, SONET framing structure, recited in col. 10, lines 25-40); **regarding claim 33**, the device (fig. 1, Packet Switched

Communication Apparatus, recited in col. 6, lines 17-27), wherein the switching matrix (fig. 1, Crossbar Switch (nxn)10, recited in col. 6, lines 17-41) is optical (fig. 2B, SONET framing structure, recited in col. 10, lines 25-40)

Moriwaki et al. discloses all the claimed limitation with the exception of being silent with regard to the following features: regarding claim 27, queues with priority.

However, Sakamoto et al. in the same field of endeavor discloses the following features: **regarding claim 27**, queues (fig. 21, Input Interfaces 3, Input Buffer 121, recited in col. 6, lines 35-49) with priority ("priority scheduling of packets", recited in col. 6, lines 35-49). Therefore, it would have been obvious to one of ordinary skills in the art at the time the invention was made to modify the features of Moriwaki et al. by using features as taught by Sakamoto et al. in order to provide priority queuing and dequeuing of packets (See Col. 8, lines 21-29 for motivation).

13. **Claim 31** is rejected under 35 U.S.C. 103(a) as being unpatentable over Moriwaki et al (US 6,999,413 B2) in view of Sakamoto et al (US 6,836,479 B1) as applied to claim27 above and further view of Miles et al (US 6,665,495 B1).

Regarding claim 31, Moriwaki et al. discloses the device as recited in above paragraph.

Moriwaki et al. and Sakamoto are silent with regard to the following features: wherein the maximum frame size is selected based on at least some subset of configuration time of data path, scheduling time for scheduler, and complexity of scheduling algorithms.

However, Miles et al. in the same field of endeavor discloses: wherein the maximum frame size ("super packets", recited in col. 7, lines 27-33) is selected based on

at least some subset of configuration time ("selected time and scheduling pattern", recited in col. 36-48) of data path ("placing of packet on the ingress links a time slots", recited in col. 14, lines 32-55), scheduling time for scheduler ("the controller schedules super packets based on scheduled algorithm", recited in col. 3, lines 29-31), and complexity of scheduling algorithms ("contention among the plurality of super packets in the transmission between the optical switch fabric and the egress units", recited in col. 3, lines 15-23). Therefore, it would have been obvious to one of ordinary skill in the art at time the invention was made to modify the features of Moriwaki et al. with Sakamoto et al. by using features as taught by Miles et al. in order to provide packet aggregations and non-blocking of optical data (See Col. 2, lines 65- col. 3, lines 9 for motivation).

14. **Claim 35** is rejected under 35 U.S.C. 103(a) as being unpatentable over Moriwaki et al (US 6,999,413) in view of Dell et al (US 2002/0085578 A1).

Regarding claim 35, Moriwaki et al. discloses the device (fig. 1, Packet Communication Apparatus, recited in col. 6, lines 17-27).

Moriwaki et al. discloses all the claimed limitation with the exception of being silent with regard to the following features: wherein a pipeline schedule is implemented that includes at least some subset of said ingress interface modules forming and transmitting requests to said scheduler, scheduler computing a schedule based on the requests, said scheduler transmitting grants to associated ingress interface modules and configuring said switching matrix, and said ingress interface modules transmitting the frames in response to the grants.

However, Dell et al (US 2002/0085578 A1) in the same field of endeavor discloses: wherein a pipeline schedule (fig. 3, see, Plural Stages 1, 2,3, recited in

paragraph 0051, paragraph 0014, lines 1-13) is implemented that includes at least some subset of said ingress interface modules (fig. 2, Ingress Line cards 202, recited in paragraph 0048, lines 1-6) forming and transmitting requests ("successful request", recited in paragraph 0085, lines 9-14) to said scheduler (fig. 4, Scheduler 418, recited in paragraph 0068, lines 1-6), scheduler (fig. 4, Scheduler 418, recited in paragraph 0068, lines 1-6) computing a schedule based on the requests ("computes of schedule every clock cycle by the scheduler", recited in paragraph 0112), said schedule (fig. 4, Scheduler 418, recited in paragraph 0068, lines 1-6) transmitting grants ("granted request then the Grant signal is fed", recited in paragraph 0068, lines 6-11) to associated ingress interface modules (fig. 2, Ingress Line cards 202, recited in paragraph 0048, lines 1-6) and configuring said switching matrix (fig. 2, Switching Fabric modules 201, recited in paragraph 0047, lines 1-9), and said ingress interface modules (fig. 2, Ingress Line cards 202, recited in paragraph 0048, lines 1-6) transmitting the frames ("transmitted cells to the crossbar devices", recited in paragraph 0118) in response to the grants ("granted request then the Grant signal is fed", recited in paragraph 0068, lines 6-11). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the features of Moriwaki et al. by using features as taught by Dell et al. in order to provide stage switching of network traffic from sources to a plurality of destinations and quality of service (See paragraphs 0011, 0013 for motivation).

14. **Claim 36** is rejected under 35 U.S.C. 103(a) as being unpatentable over Moriwaki et al (6,999413 B2) in view of Tornetta et al (US 6,950,448 B2).

Regarding claim 36, Moriwaki et al. discloses the (fig. 1, Packet Switched Communication Apparatus, recited in col. 6, lines 17-27) and the switching matrix, the

scheduler as recited in above paragraph, align configuration changes ("adjust of the timing", recited in col. 8, lines 36-41), and maintains an uninterrupted data stream to the egress interface modules by transmitting an idle stream when no frames are being transmitted ("supply of idle block to the line interface", recited in col. 11, lines 34-45).

Moriwaki et al. discloses all the claimed limitation with the exception of being silent with regard to the following features: wherein said switching matrix extracts a clock from frames received, re-times the frames to a common internal clock domain, aligns any configuration changes provided by said scheduler to the boundaries of the frames, and maintains an uninterrupted data stream to the egress interface modules by transmitting an idle stream when no frames are being transmitted.

However, Tornetta et al. in the same field of endeavor discloses the following features: **regarding claim 36**, wherein said switching matrix (fig. 4, Switching Matrix 15, extracts a clock from frames received ("generates of serial clock", recited in col. 5, lines 55-59), re-times the frames to a common internal clock domain ("receiver use of transition to phase align recovered clock with the data", recited in col. 5, lines 60-64). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the features of Moriwaki et al. by using features as taught by Tornetta et al. in order to extract/recover clock signals from the received frames (See Col. 5, lines 9-25 for motivation).

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Kim et al (US 7,245,641 B2) , and Reches et al (US 2002/0110086 A1).

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Candal Elpenord whose telephone number is (571) 270-3123. The examiner can normally be reached on Monday through Friday 7:30AM to 5:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kwang Bin Yao can be reached on (571) 272-3182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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CE

KWANG BIN YAO
SUPERVISORY PATENT EXAMINER

Continuation of Attachment(s) 3). Information Disclosure Statement(s) (PTO/SB/08), Paper No(s)/Mail Date :14 January 2005, 02 November 2007.